PATENT ABSTRACTS OF JAPAN

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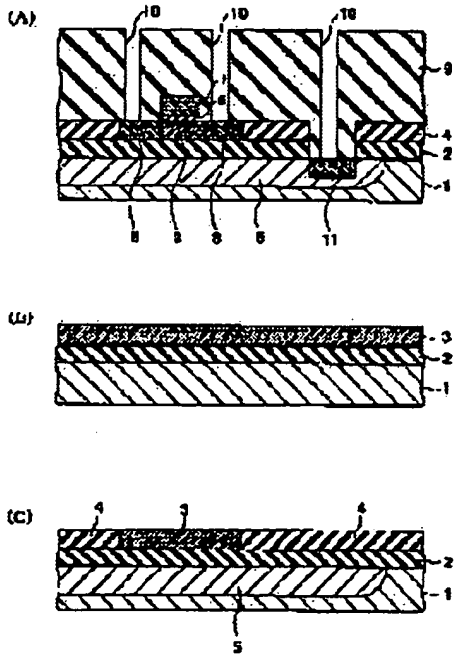
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a manufacture of a semiconductor device capable of forming a semiconductor device and a substrate contact on an SOI substrate by a simplified process.

SOLUTION: This manufacture of a semiconductor device for forming a transistor on a substrate composed of a first semiconductor layer 1, an insulator layer 2 and a second semiconductor layer 3 has a step of forming an element isolation region 4 in the second semiconductor layer 3, a step of forming an opening reaching the first semiconductor layer 1 in the element isolation region 4, a step of forming a gate electrode 7 on the second semiconductor layer 3, a step of introducing impurities in the second semiconductor layer 3 and the opening to form a source/drain region 8 in the second semiconductor layer 3 and a high-concentration impurity diffused region 11 in the first semiconductor layer 2 (5), a step of forming an interlayer insulating film 9, and a step of forming a contact hole 10 in the interlayer insulating film 9.



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[Date of request for examination]

comprises an N-channel MOSFET 52 and a P-channel MOSFET 54 formed above a buried silicon oxide layer 56. The buried oxide layer (BOX) 56 is formed on a silicon substrate 80. Surrounding the MOSFETs 52 and 54 is a field oxide region 58 (FOX).

The N-channel MOSFET 52 includes a polycrystalline silicon gate 60, a N^+ source region 62 and a N^+ drain region 64. Between the source region 62 and the drain region 64, and below the gate 60, a P^- region 66 is provided. In Fig. 3, the source region 62 and the drain region 64 are shown to be shallower than the buried oxide layer, but in practice, the source region 62 and the drain region 64 may extend down to the buried oxide layer, as shown in Figure 4. Located below the buried oxide layer 56 and below the P^- region 66 is a region 67 which is of the same conductivity type i.e. P as the channel region 66. In the illustrated MOSFET 52, the region 67 is part of a P-well 68 which is formed above and below i.e. divided by the buried oxide layer 56. Similarly, the P-channel MOSFET 54 includes a polycrystalline silicon gate 70, a P^+ source region 72 and a P^+ drain region 74. Between the source region 72 and the drain region 74, and below the gate 70, an N^- region 76 is provided. The source region 72 and the drain region 74 are shown to be shallower than the buried oxide layer 56, but in practice, the source region 72 and the drain region 74 may extend down to the buried oxide layer 56 as shown in Figure 4. Located below the buried oxide layer 56 and below the N^- region 76 is a region 77 which is of the same conductivity type i.e. N as the channel region 76. In the illustrated MOSFET 54, the region 77 is part of an N-well 78 which is formed above and below i.e. divided by the buried oxide layer 56. It should be obvious to one skilled in the art, that other planar MOSFET designs can be applied into this well formation method e.g. gates may be metal, polycide or salicide.

By using the standard bulk CMOS P-well and N-well masks, the wells 68 and 78 are implanted both above the buried oxide layer 56 and below the buried oxide layer 56 in the bulk region. In the embodiment illustrated in Figure 3, the bulk region is an N, or P, substrate 80. One or more energy levels may be used for the ion implant of the wells 68, 78 after the buried oxide layer 56 is formed. In this regard, implant energies of 500 keV to several megavolts may be used. Alternatively, the wells 68, 78 may be formed using normal 100 keV or less implant energies followed by heavy oxygen implant for the formation of the buried oxide layer 56 using the SIMOX technique. The well drive then takes place during the oxygen implant anneal at approximately 1300□